

FLOATING GATE MEMORY STRUCTURES AND FABRICATION METHODS

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5 ABSTRACT OF THE DISCLOSURE

Dielectric regions (210) are formed on a semiconductor substrate between active areas of nonvolatile memory cells. The top portions of the dielectric region sidewalls are etched to recess the top portions laterally away from the active areas. Then a conductive layer is deposited to form the floating gates (410). The recessed portions of the dielectric
10 sidewalls allow the floating gates to be wider at the top. The gate coupling ratio is increased as a result. Other features are also provided.